

ABSTRACT

Alternating current is used to sense a logic state of a memory cell that has a resistive memory element. The memory element can be in an array and a memory device can include the array and peripheral circuitry for reading or sensing each memory cell in the array. The peripheral circuitry can include a clock/control circuit providing a control signal, which controls when a row of memory cells are sensed, a switching circuit for receiving a cellplate count signal and a bit count signal provided by the clock/control circuit, a cellplate line signal and a bit line signal from the memory cell, the switching circuit producing a first output signal and a second output signal, wherein one of the first output signal and the second output signal is at a supply voltage and the other of the first output signal and the second output signal alternates polarity with each sensing operation and a comparison circuit receiving the first output signal and the second output signal and outputting a signal corresponding to the logic state of the memory cell.